ESD (HUMAN BODY MODE) TEST REPORT

Company ：无锡纳瓦特电子有限公司

Address ：无锡市滨湖区五湖大道**11**号蠡湖科创中心**A**栋**11**楼

Model Name ：**NV32F100**

Date Received ：May 13,2015

Date Tested ：May 13,2015

TESTING LABORATORY IS ACCREDITED BY:

IEC/IECQ 17025 certificate of independent test laboratory approval

CB Certificate No.: 1.72.0031/B IECQ Certificate No.: IECQ-L NSAIUS 09.0005

ISO 9001 certificate is approved by TUV CERT certification body of TUV NORD Cert GmbH

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Jianbo Song	Jianbo Song	2015/5/13
Approving Manager	Alston Wang	Alston Wang	2015/5/13

Note：

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.

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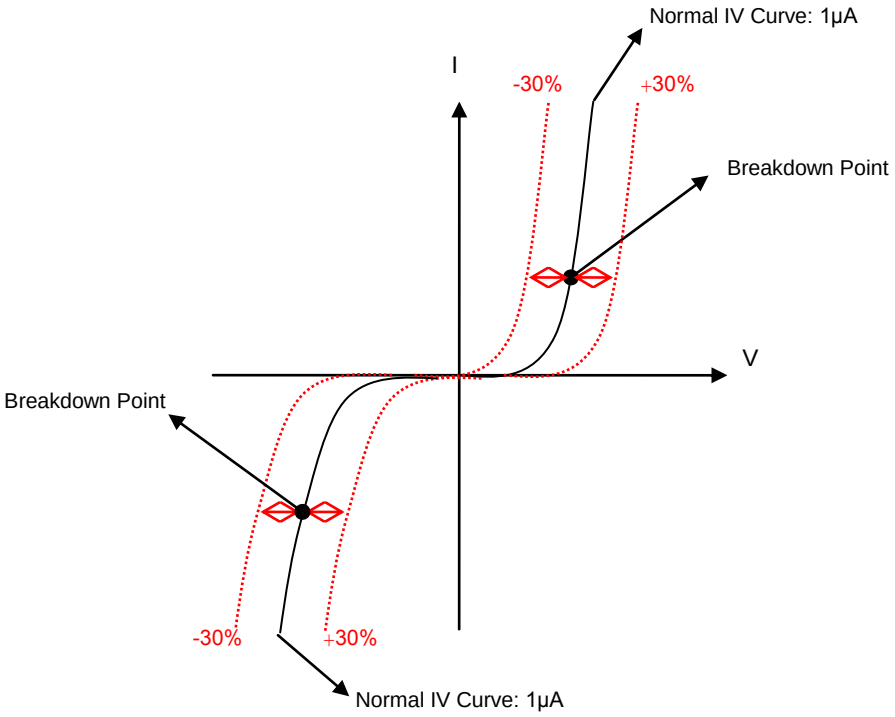
1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	: 无锡纳瓦特电子有限公司
DEVICE NAME	: NV32F100
PACKAGED / PIN COUNT	: LQFP64
REFERENCE DOCUMENT	: MIL-STD-883H Method 3015.8 Zap **3** pulse(s), Interval: **1.0** Sec.
TEST VOLTAGE	: 4500V(±), 6000V(±),8000V(±);
SAMPLE QUANTITY	: 5 pcs
FAILURE CRITERIA	: FOR V CHANGE AT 1μA ±30%

※ Failure Judgment: IV curve shift over 1μA±30% at breakdown point.



2. ESD (HUMAN BODY MODE) TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER 7/4	0008189	July30, 2014	July 29, 2015

2.2 LABORATORY AMBIENCE CONDITION

Temperature：23±5°C

Relative humidity：55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on MIL-STD-883H Method 3015.8

2.4 TEST CONDITION

All other pins to VSS (+/-)
All other pins to VDD (+/-)
All other pins to VDDA (+/-)
IO TO IO (+/-)
Step:4500V

All other pins to VSS (+/-)
All other pins to VDD (+/-)
All other pins to VDDA (+/-)
IO TO IO (+/-)
Step:6000V

All other pins to VSS (+/-)
All other pins to VDD (+/-)
All other pins to VDDA (+/-)
IO TO IO (+/-)
Step:8000V

2.5 SUMMARY OF TEST

Test Model : HBM	**ESD Sensitivity Passed : +/-8000V**		**MIL-STD Classification Class : 3**
Test condition	Sample Quantity	Passed Volts	**Class 0 : < 250V.** **Class 1A : ≧ 250V , <500V** **Class 1B : ≧ 500V , <1000V** **Class 1C : ≧1000V , <2000V** **Class 2 : ≧2000V , <4000V** **Class 3A : ≧4000V , <8000V** **Class 3B : ≧8000V**
All other pins to VSS (+/-) All other pins to VDD (+/-) All other pins to VDDA (+/-) IO TO IO (+/-) Step:4500V	3	+/-4500V	
All other pins to VSS (+/-) All other pins to VDD (+/-) All other pins to VDDA (+/-) IO TO IO (+/-) Step:6000V	1	+/-6000V	
All other pins to VSS (+/-) All other pins to VDD (+/-) All other pins to VDDA (+/-) IO TO IO (+/-) Step:8000V	1	+/-8000V	

Group	**Pins**
IO	1-6,9,11-12,14-39,42-64
VDD	7,41
VDDA	8
VSS	10,13,40

2.6 CONTENTS OF TEST

No	1		
All other pins to VSS (+/-) All other pins to VDD (+/-) All other pins to VDDA (+/-) IO TO IO (+/-) Step:4500V			
Tested Pins	Sample No. & Failed Volt		
	#1	#2	#3
1	PASS(4500V)	PASS(4500V)	PASS(4500V)
2	PASS(4500V)	PASS(4500V)	PASS(4500V)
3	PASS(4500V)	PASS(4500V)	PASS(4500V)
4	PASS(4500V)	PASS(4500V)	PASS(4500V)
5	PASS(4500V)	PASS(4500V)	PASS(4500V)
6	PASS(4500V)	PASS(4500V)	PASS(4500V)
7	PASS(4500V)	PASS(4500V)	PASS(4500V)
8	PASS(4500V)	PASS(4500V)	PASS(4500V)
9	PASS(4500V)	PASS(4500V)	PASS(4500V)
10	PASS(4500V)	PASS(4500V)	PASS(4500V)
11	PASS(4500V)	PASS(4500V)	PASS(4500V)
12	PASS(4500V)	PASS(4500V)	PASS(4500V)
13	PASS(4500V)	PASS(4500V)	PASS(4500V)
14	PASS(4500V)	PASS(4500V)	PASS(4500V)
15	PASS(4500V)	PASS(4500V)	PASS(4500V)
16	PASS(4500V)	PASS(4500V)	PASS(4500V)
17	PASS(4500V)	PASS(4500V)	PASS(4500V)
18	PASS(4500V)	PASS(4500V)	PASS(4500V)
19	PASS(4500V)	PASS(4500V)	PASS(4500V)
20	PASS(4500V)	PASS(4500V)	PASS(4500V)
21	PASS(4500V)	PASS(4500V)	PASS(4500V)
22	PASS(4500V)	PASS(4500V)	PASS(4500V)
23	PASS(4500V)	PASS(4500V)	PASS(4500V)
24	PASS(4500V)	PASS(4500V)	PASS(4500V)
25	PASS(4500V)	PASS(4500V)	PASS(4500V)
26	PASS(4500V)	PASS(4500V)	PASS(4500V)
27	PASS(4500V)	PASS(4500V)	PASS(4500V)
28	PASS(4500V)	PASS(4500V)	PASS(4500V)
29	PASS(4500V)	PASS(4500V)	PASS(4500V)
30	PASS(4500V)	PASS(4500V)	PASS(4500V)
31	PASS(4500V)	PASS(4500V)	PASS(4500V)
32	PASS(4500V)	PASS(4500V)	PASS(4500V)
33	PASS(4500V)	PASS(4500V)	PASS(4500V)
34	PASS(4500V)	PASS(4500V)	PASS(4500V)
35	PASS(4500V)	PASS(4500V)	PASS(4500V)
36	PASS(4500V)	PASS(4500V)	PASS(4500V)
37	PASS(4500V)	PASS(4500V)	PASS(4500V)
38	PASS(4500V)	PASS(4500V)	PASS(4500V)
39	PASS(4500V)	PASS(4500V)	PASS(4500V)
40	PASS(4500V)	PASS(4500V)	PASS(4500V)
41	PASS(4500V)	PASS(4500V)	PASS(4500V)

42	PASS(4500V)	PASS(4500V)	PASS(4500V)
43	PASS(4500V)	PASS(4500V)	PASS(4500V)
44	PASS(4500V)	PASS(4500V)	PASS(4500V)
45	PASS(4500V)	PASS(4500V)	PASS(4500V)
46	PASS(4500V)	PASS(4500V)	PASS(4500V)
47	PASS(4500V)	PASS(4500V)	PASS(4500V)
48	PASS(4500V)	PASS(4500V)	PASS(4500V)
49	PASS(4500V)	PASS(4500V)	PASS(4500V)
50	PASS(4500V)	PASS(4500V)	PASS(4500V)
51	PASS(4500V)	PASS(4500V)	PASS(4500V)
52	PASS(4500V)	PASS(4500V)	PASS(4500V)
53	PASS(4500V)	PASS(4500V)	PASS(4500V)
54	PASS(4500V)	PASS(4500V)	PASS(4500V)
55	PASS(4500V)	PASS(4500V)	PASS(4500V)
56	PASS(4500V)	PASS(4500V)	PASS(4500V)
57	PASS(4500V)	PASS(4500V)	PASS(4500V)
58	PASS(4500V)	PASS(4500V)	PASS(4500V)
59	PASS(4500V)	PASS(4500V)	PASS(4500V)
60	PASS(4500V)	PASS(4500V)	PASS(4500V)
61	PASS(4500V)	PASS(4500V)	PASS(4500V)
62	PASS(4500V)	PASS(4500V)	PASS(4500V)
63	PASS(4500V)	PASS(4500V)	PASS(4500V)
64	PASS(4500V)	PASS(4500V)	PASS(4500V)

No	2
All other pins to VSS (+/-) All other pins to VDD (+/-) All other pins to VDDA (+/-) IO TO IO (+/-) Step:6000V	
Tested Pins	Sample No. & Failed Volt
	#4
1	PASS(6000V)
2	PASS(6000V)
3	PASS(6000V)
4	PASS(6000V)
5	PASS(6000V)
6	PASS(6000V)
7	PASS(6000V)
8	PASS(6000V)
9	PASS(6000V)
10	PASS(6000V)
11	PASS(6000V)
12	PASS(6000V)
13	PASS(6000V)
14	PASS(6000V)
15	PASS(6000V)
16	PASS(6000V)
17	PASS(6000V)
18	PASS(6000V)
19	PASS(6000V)
20	PASS(6000V)
21	PASS(6000V)
22	PASS(6000V)
23	PASS(6000V)
24	PASS(6000V)
25	PASS(6000V)
26	PASS(6000V)
27	PASS(6000V)
28	PASS(6000V)
29	PASS(6000V)
30	PASS(6000V)
31	PASS(6000V)
32	PASS(6000V)
33	PASS(6000V)
34	PASS(6000V)
35	PASS(6000V)
36	PASS(6000V)
37	PASS(6000V)
38	PASS(6000V)
39	PASS(6000V)
40	PASS(6000V)
41	PASS(6000V)

42	PASS(6000V)
43	PASS(6000V)
44	PASS(6000V)
45	PASS(6000V)
46	PASS(6000V)
47	PASS(6000V)
48	PASS(6000V)
49	PASS(6000V)
50	PASS(6000V)
51	PASS(6000V)
52	PASS(6000V)
53	PASS(6000V)
54	PASS(6000V)
55	PASS(6000V)
56	PASS(6000V)
57	PASS(6000V)
58	PASS(6000V)
59	PASS(6000V)
60	PASS(6000V)
61	PASS(6000V)
62	PASS(6000V)
63	PASS(6000V)
64	PASS(6000V)

No	3
All other pins to VSS (+/-) All other pins to VDD (+/-) All other pins to VDDA (+/-) IO TO IO (+/-) Step:8000V	
Tested Pins	Sample No. & Failed Volt
	#2-8K
1	PASS(8000V)
2	PASS(8000V)
3	PASS(8000V)
4	PASS(8000V)
5	PASS(8000V)
6	PASS(8000V)
7	PASS(8000V)
8	PASS(8000V)
9	PASS(8000V)
10	PASS(8000V)
11	PASS(8000V)
12	PASS(8000V)
13	PASS(8000V)
14	PASS(8000V)
15	PASS(8000V)
16	PASS(8000V)
17	PASS(8000V)
18	PASS(8000V)
19	PASS(8000V)
20	PASS(8000V)
21	PASS(8000V)
22	PASS(8000V)
23	PASS(8000V)
24	PASS(8000V)
25	PASS(8000V)
26	PASS(8000V)
27	PASS(8000V)
28	PASS(8000V)
29	PASS(8000V)
30	PASS(8000V)
31	PASS(8000V)
32	PASS(8000V)
33	PASS(8000V)
34	PASS(8000V)
35	PASS(8000V)
36	PASS(8000V)
37	PASS(8000V)
38	PASS(8000V)
39	PASS(8000V)
40	PASS(8000V)
41	PASS(8000V)

42	PASS(8000V)
43	PASS(8000V)
44	PASS(8000V)
45	PASS(8000V)
46	PASS(8000V)
47	PASS(8000V)
48	PASS(8000V)
49	PASS(8000V)
50	PASS(8000V)
51	PASS(8000V)
52	PASS(8000V)
53	PASS(8000V)
54	PASS(8000V)
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56	PASS(8000V)
57	PASS(8000V)
58	PASS(8000V)
59	PASS(8000V)
60	PASS(8000V)
61	PASS(8000V)
62	PASS(8000V)
63	PASS(8000V)
64	PASS(8000V)